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| 10/727,440 | 12/04/2003 | Ken G. Pomaranski | 200209695-1 | 6842 |

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| EXAMINER | |
|---|---|
| BUI, BRYAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2863 | |

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/727,440 | POMARANSKI ET AL. |
| | Examiner | Art Unit |
| | Bryan Bui | 2863 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-19* is/are allowed.

6)☒ Claim(s) *1-9,11 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicants' papers filed on 10/31/2005 have been received and entered. Claims 1, 5, 6, 13 and 17 have been amended. Claims 10, 12, and 20 have been cancelled. Claims 1-9, 11, and 13-19 are pending in the application.

2. Applicants' remarks have been fully considered.

3. It is noted that the term "de-allocated" and re-allocated" as recited in claim 13 is considered as inherently known in the computer technology (Microsoft press Computer Dictionary, third edition) by not reserve a resource/to free previously allocated memory (de-allocated); and the allocation of memory to a process or program or reserve a resource (re-allocated).

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 13, applicants claim a method performed by an interconnect test module in a computer system comprising the limitations of steps which do not point out the claim subject matter that applicants want to refer to. For instant, the figures submitted do not relates to this performance. Further, what is the implementation of using an interconnect test module in this claim to represent for the application? If it apply for performance the component being de-allocated from use by the operating system, it does not show any implementation of the function of the performance a test

as mentioned, it likes a processor (as test module) and an operating system admitted in computer system for supporting the process by booting/rebooting the computer system as commonly known in field of the computer system or disclosed in the prior art (6757803) for de-allocated memory (this is not good for the system), and the present of application clearly show the interconnect test module corresponding between test signal and test pattern of components. Therefore, the limitations of claim 13 do not clarify the subject matter on what applicant regards in the invention.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al (US 6,757,803).

With respect to claims 13-14, Lin et al teach a computer system having an interconnect test module (figures 1, 9, with a processor (as test module) and an operating system admitted in computer system for supporting the process by booting/rebooting the computer system as commonly known in field of the computer system) comprising causing a component (processor/memory/storage, etc) coupled to an interconnect to be de-allocated from use by an operating system and performing a

test on the interconnect causing the component to be re-allocated to use by the operating system subsequent to performing the test (column 1, lines 36-56, column 9, lines 5-29 and column 11, lines 16-25); notifying the operating system in response to detecting an error in performance the test (column 7, lines 7-20).

With respect to claims 15-16, Lin et al teach reporting results of the test to the operating system (column 4, lines 1-17); performing the test on the interconnect by providing test patterns on the interconnect (column 4, lines 39-53, column 10, line 45 to column 11, line 33).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-9, 11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coyle et al (US 6609221) in view of Lin et al (US 6757803).

With respect to claims 1-6, Coyle et al teach a computer system having an interconnect test module comprising a processor configured to cause an operating system to be booted and interconnect (figure 1, column 5, lines 13-29), a first test unit (first test device) coupled to the interconnect, and a second test unit (second test device) coupled to the interconnect (figure 1, column 5, lines 13-29); wherein the first test unit is configured to provide a test pattern to the second test unit on the interconnect in response to a signal from the operating system (column 5, lines 33-41,

column 6, lines 1-8); a second test unit is configured to detect an error in the interconnect in response to receiving the test pattern and notifying (indicating, reporting) the operating system in response to detecting an error (column 6, lines 5-33 ). Coyle et al does not mention a step of causing a component coupled to be de-allocated from use by an operating system. Line et al, however teach these limitations (column 1, lines 36-56, column 9, lines 5-29, and column 11, lines 16-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Coyle et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated (column 1, lines 6-13)/ or providing a de-allocated memory in accordance with the ordinary and usual methods of de-allocation of memory by a process as disclosed in Lin (column 11, lines 21-25).

With respect to claims 7-9, 11 Coyle et al teach the first component comprises a processor, and wherein the second component comprises a controller coupled to the processor and controller include a system controller, and controller comprises a memory controller (column 5, lines 12-38, column 11,lines 31-50); wherein the first component comprises an input/output (I/O) controller, and the second component comprises an input/output (I/O) device coupled to the I/O controller through an expansion slot (column 12, lines 7-27, further see Microsoft Press, Computer Dictionary,

Third Edition "expansion slot" as inherent known to system bus for communicate as a socket in the computer system).

With respect to claims 13-14, Coyle et al teaches a computer system having an interconnect test module comprising a processor configured to cause an operating system (figure 1, column 5, lines 13-29), performing a test on the interconnect through the test units (first and second test devices) coupled to the interconnect (figure 1, column 5, lines 13-29); and notifying (indicating, reporting) the operating system in response to detecting an error (column 6, lines 5-33). Coyle et al does not mention a step of causing a component coupled to an interconnect to be de-allocated from use by an operating system and causing the component to be re-allocated to use by the operating system subsequent to performing the test. Lin et al, however teach these limitations (column 9, lines 23-29, and column 10, lines 15-23, column 11, lines 16-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Coyle et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system, and the operating system causing the expansion slot (socket in interface bus of the computer system) as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated (column 1, lines 6-13)/ or providing a de-allocated memory in accordance with the ordinary and usual methods of de-allocation of memory by a process as disclosed in Lin et al (column 11, lines 21-25).

With respect to claims 15-16, Coyle et al teach reporting results of the test to the operating system (column 9, lines 9-19); performing the test on the interconnect by providing test patterns on the interconnect (column 9, lines 24-43).

10. Claims 1-9, 11 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al (US 6965648) in view of Lin et al (US 6757803).

With respect to claims 1-6, Smith et al teach a computer system having an interconnect test module (figure 1, items 18A, 18B, 20A, 20B) comprising a processor configured to cause an operating system to be booted and interconnect (figure 1, an interconnect BIST (IBIST) control circuit 14, column 6, lines 38+), a first component that comprises a first test module (figure 1, items 12A, 18A), a second component that comprises a second test module (figure 1, items 12B, 20A) an interconnect coupling the first component and the second component (figure 1, item 16A); wherein the first test unit is configured to provide a first test signal to operating system to provide controlled signal to second component (column 1, lines 45+; column 4, lines 10+), and wherein the first test module is configured to provide a first test pattern to the second test module on the interconnect in response to a second signal from the operating system and a second test unit is configured to detect an error in the interconnect in response to receiving the test pattern and notifying (indicating, indication, report) the operating system in response to detecting an error (column 3, line 52 to column 4, line 9). Smith et al does not mention of causing a second component coupled to be de-allocated from use by an operating system. Line et al, however teach these limitations (column 1, lines 36-56, column 9, lines 5-29, and column 11, lines 16-25). It would have been obvious to

one of ordinary skill in the art at the time the invention was made to modify Smith et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated (column 1, lines 6-13)/ or providing a de-allocated memory in accordance with the ordinary and usual methods of de-allocation of memory by a process as disclosed in Lin (column 11, lines 21-25).

With respect to claims 7-9, 11 Smith et al teach the first component comprises a processor, and wherein the second component comprises a controller coupled to the processor and controller include a system controller, and controller comprises a memory controller (column 6, lines 38-54); wherein the first component comprises an input/output (I/O) controller, and the second component comprises an input/output (I/O) device coupled to the I/O controller through an expansion slot (column 6, lines 38-44, further see Microsoft Press, Computer Dictionary, Third Edition for "expansion slot" as inherent known to system bus for communicate as a socket in the computer system, and definitions of peripheral interface chip and integrated circuit and chip).

With respect to claims 13-14, Smith et al teach a computer system having an interconnect test module (figure 1, items 18A, 18B, 20A, 20B) comprising a processor configured to cause an operating system to perform test and an interconnect module (figure 1, an interconnect BIST (IBIST) control circuit 14, column 6, lines 38+), an

interconnect coupling component {sic} (figure 1, item 16A); wherein the test module is configured to provide a subsequent test controlled signal to component from use by operating system (column 3, lines 52+ and column 4, lines 47+), and notifying the operating system in response to detecting error in performance the test (column 3, line 52 to column 4, line 9). Smith et al does not mention to the component to be de-allocated and re-allocated from use by an operating system. Line et al, however teach these limitations (column 1, lines 36-56, column 9, lines 5-29, and column 11, lines 16-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Smith et al' teachings to include a process to cause the component coupled to an interconnect to be de-allocated by an operating system as taught by Lin et al in order to recovery of memory in a computer system to avoiding loss of regions of memory by failure of the process to return allocated memory after finishing with it so that the region of memory can be de-allocated (column 1, lines 6-13)/ or providing a de-allocated memory in accordance with the ordinary and usual methods of de-allocation of memory by a process as disclosed in Lin (column 11, lines 21-25).

With respect to claims 15-16, Smith et al teach reporting results of the test to the operating system (column 3, line 52 to column 4, line 9); performing the test on the interconnect by providing test patterns on the interconnect (column 4, lines 47+).

***Allowable Subject Matter***

11. Claims 17-19 are allowed (the reasons for allowance that provide the limitations as mentioned in the previous office action).

***Response to Arguments***

12. Applicant's arguments filed 10/7/2005 have been fully considered but they are not persuasive.

Applicant is reminded that during patent examination, the pending claims must be "given the broadest reasonable interpretation consistent with the specification." Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969).

While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonable allowed. This means that the words of the claim must be given their plain meaning. In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). Further, the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In this instant applicant argues that the prior art of record does not teach "wherein the first test module...to a second signal from the operating system". Examiner's position is that the combination of Coyle et and Lin et al/ or combination of Smith and Lin et al apparently discloses the claimed invention as set forth above.

***Conclusion***

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BB

12/7/2005

BRYAN BUI
PRIMARY EXAMINER